Jc971 U.S. PTO
09/811435
03/20/01

Subclass	ISSUE CLASSIFICATION
Class	

BEST AVAILABLE COPY

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED ICW SBL O.A.	

(684)

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/811435	F	716/14	738	2825 2123	Decady

APPLICANTS

Michinobu Nakao
Kazumi Hatayama
Koichiro Natsume
Yoshikazu Kiyoshige

TITLE

Test method of semiconductor intergrated circuit and test pattern generator

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
	_____ (Assistant Examiner)		_____ (Date)		
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				ISSUE FEE	
				Amount Due	Date Paid
	_____ (Primary Examiner)		_____ (Date)		
☐ The terminal ____months of this patent have been disclaimed.				ISSUE BATCH NUMBER	
	_____ (Legal Instruments Examiner)		_____ (Date)		

WARNING:
The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A
(Rev. 6/99)

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM
(Attached in pocket on right inside flap)